

Fig. 1A

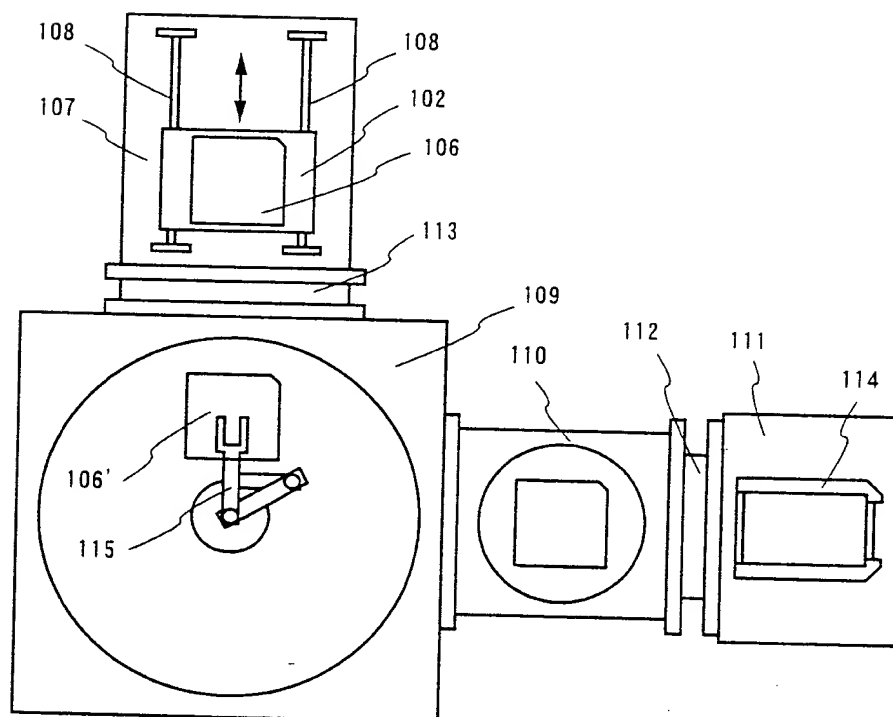


Fig. 1B

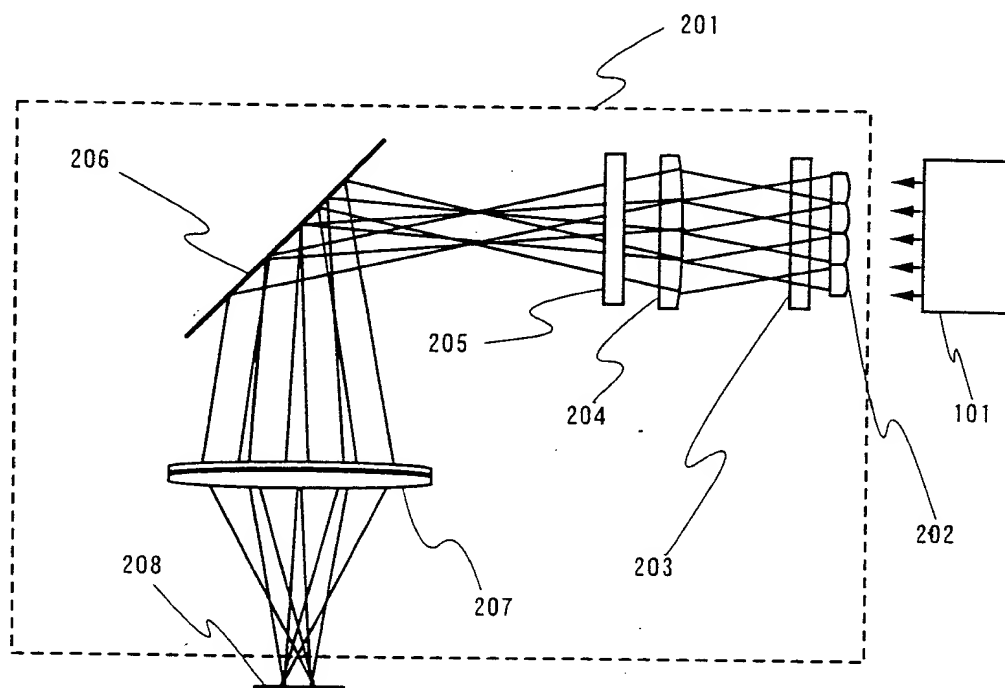


Fig. 2 A

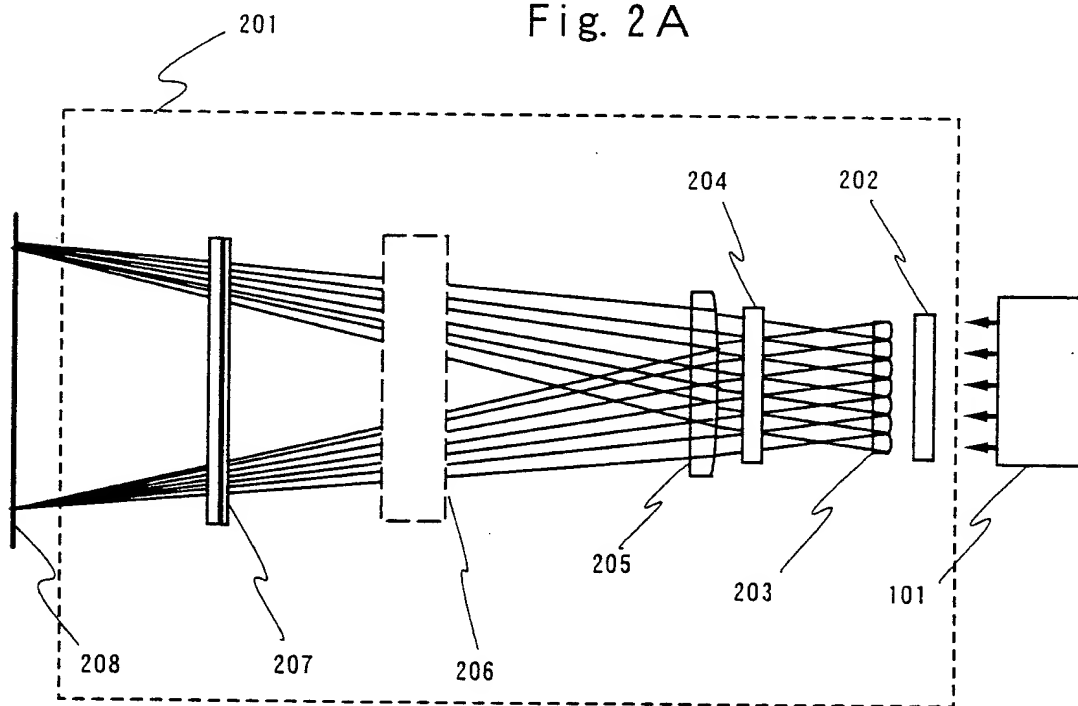


Fig. 2 B

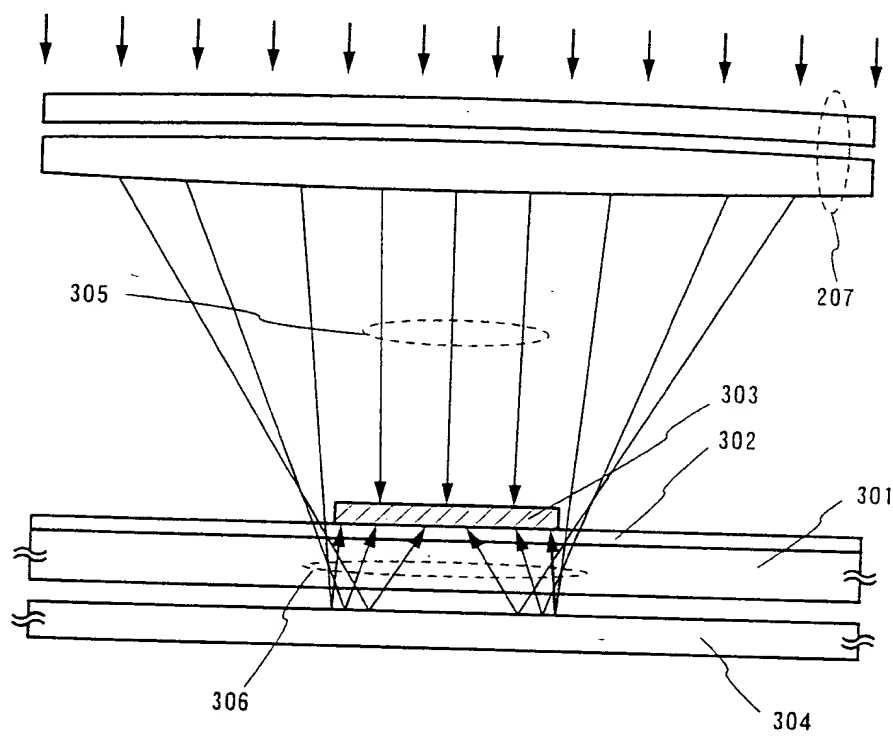


Fig. 3

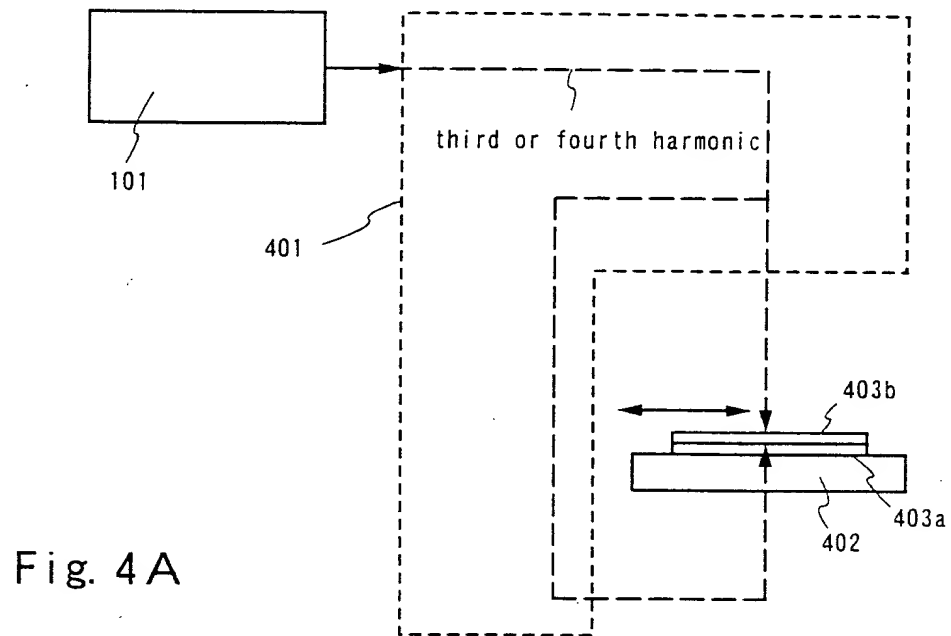


Fig. 4A

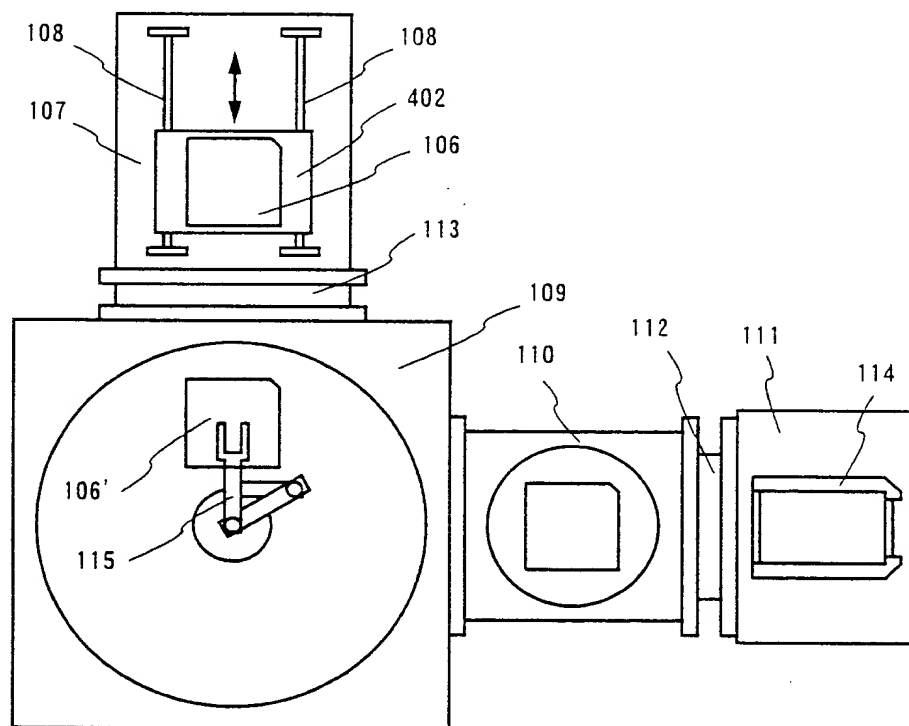


Fig. 4B

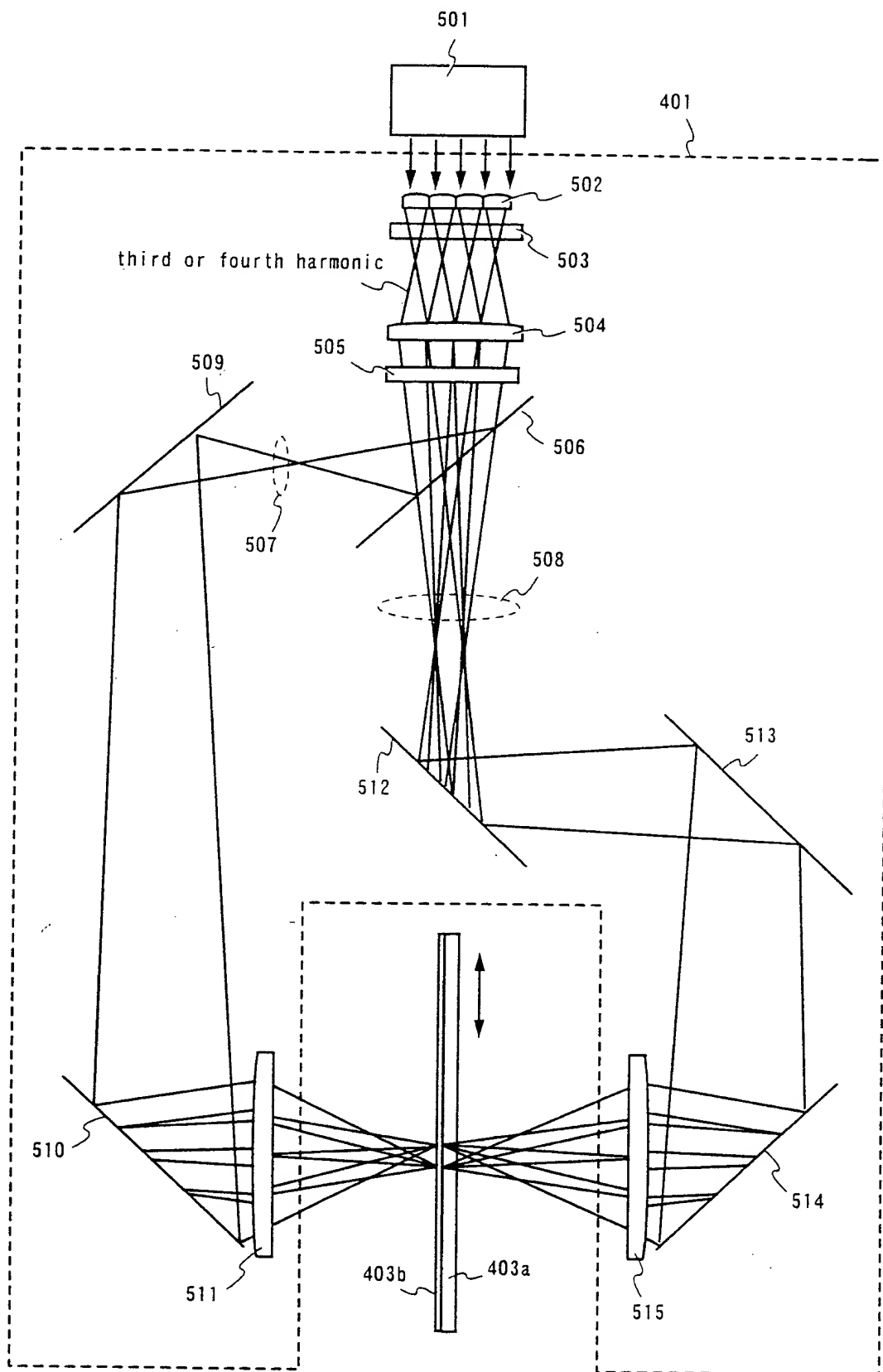


Fig. 5

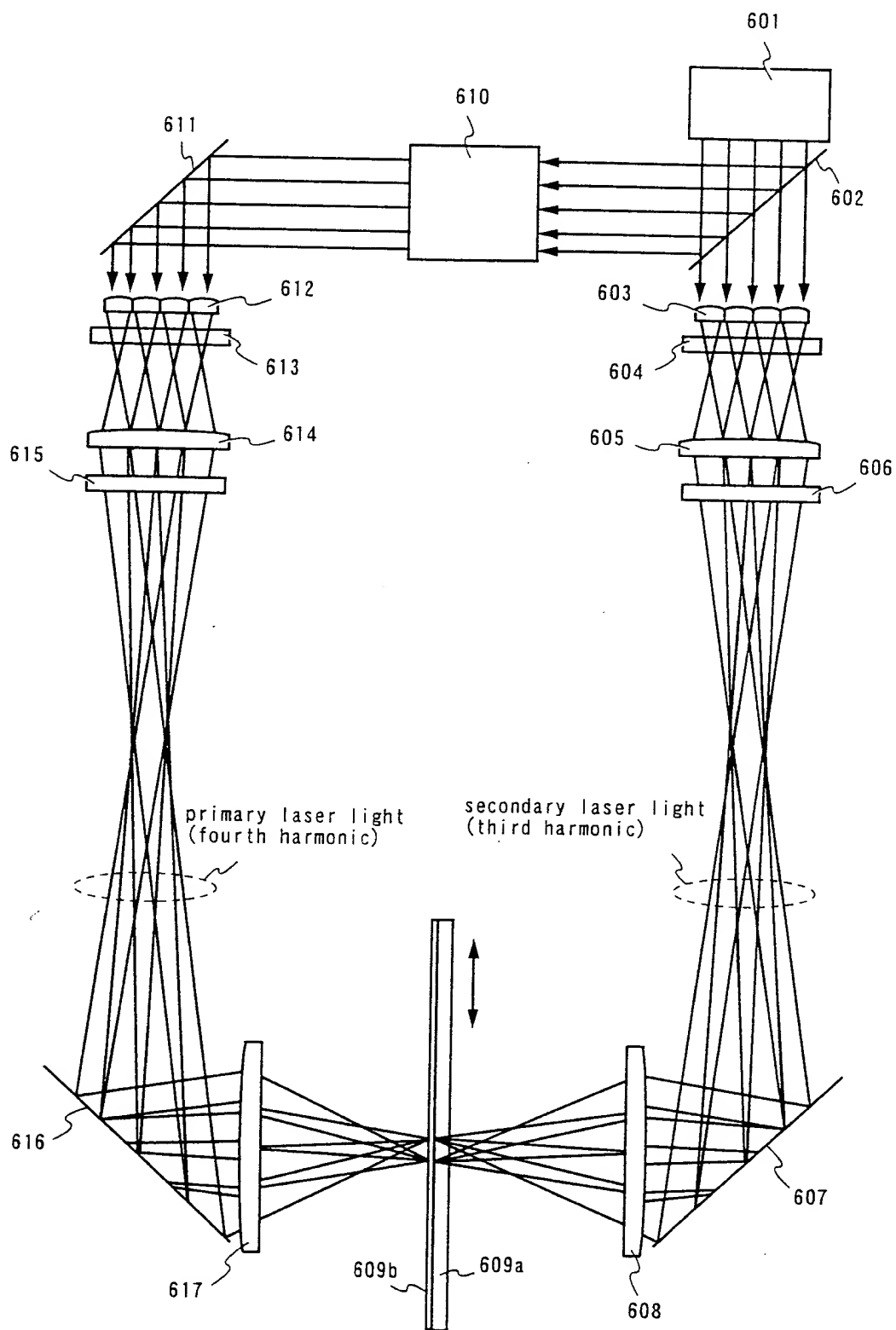


Fig. 6

Fig. 7A

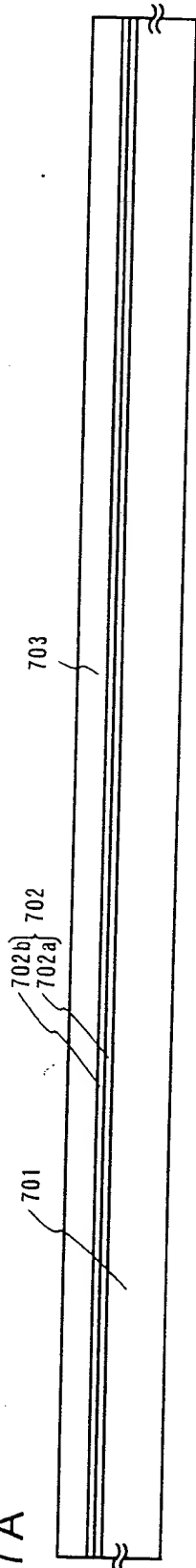


Fig. 7B

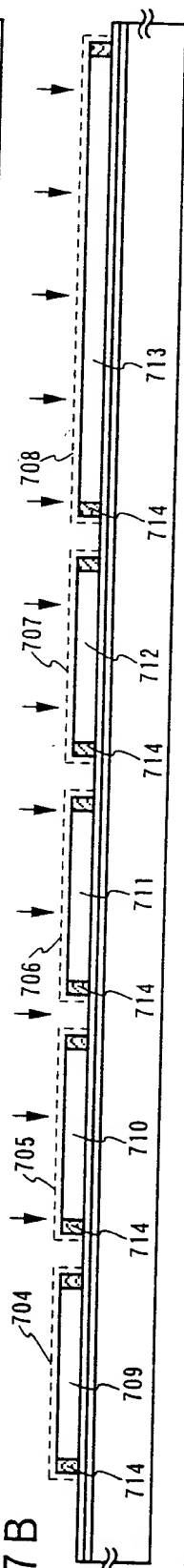


Fig. 7C

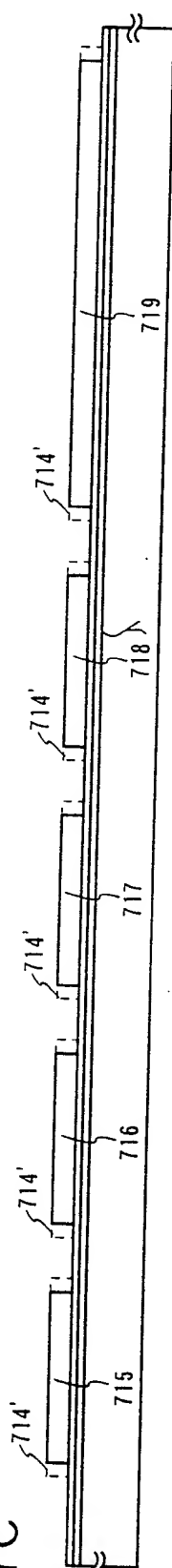


Fig. 7D

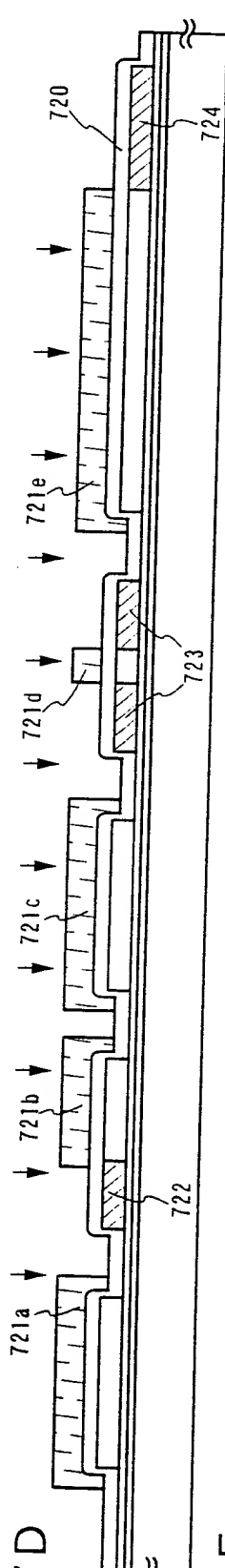


Fig. 7E

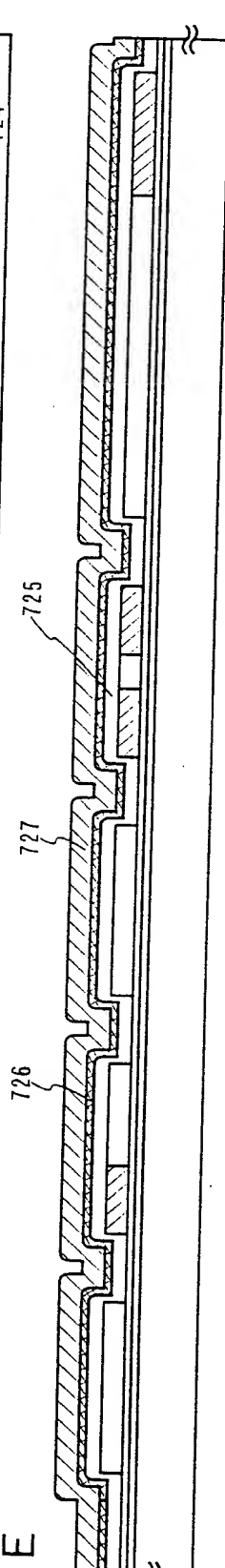


Fig. 8A

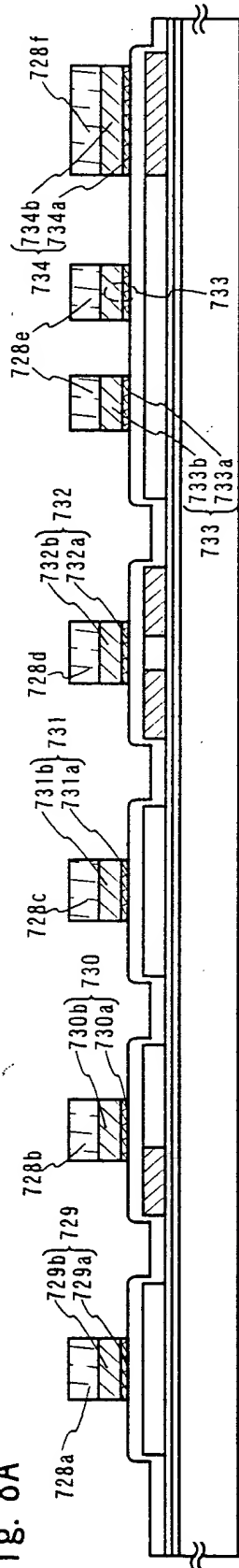


Fig. 8B

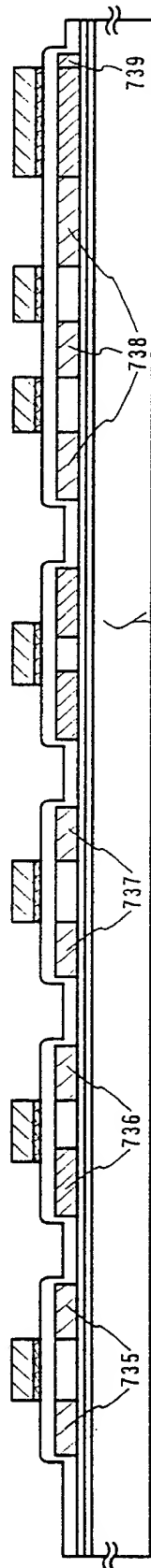


Fig. 8C

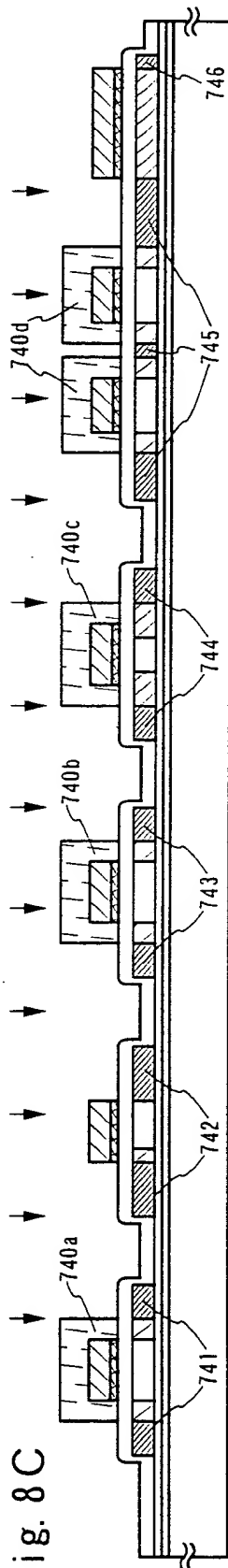


Fig. 8D

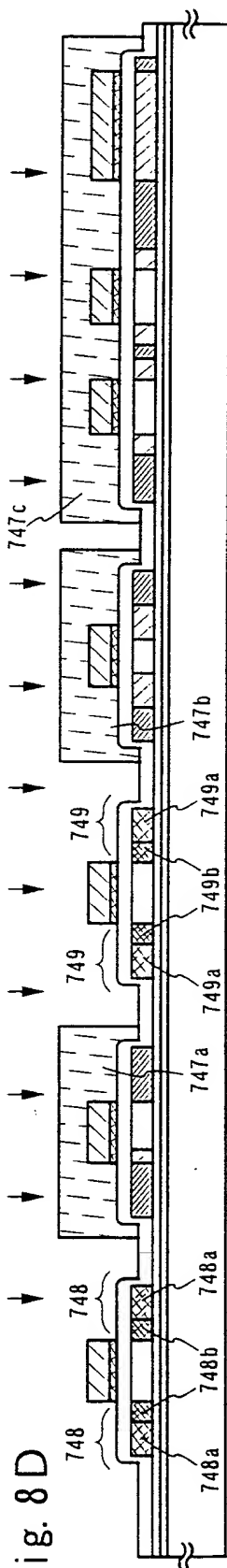


Fig. 9A

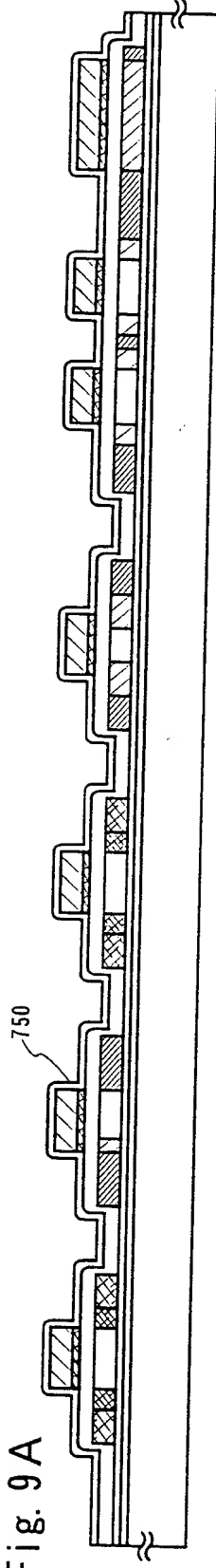


Fig. 9B

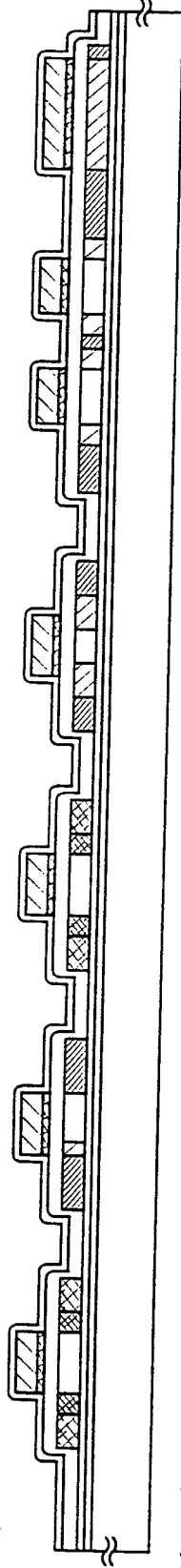


Fig. 9C

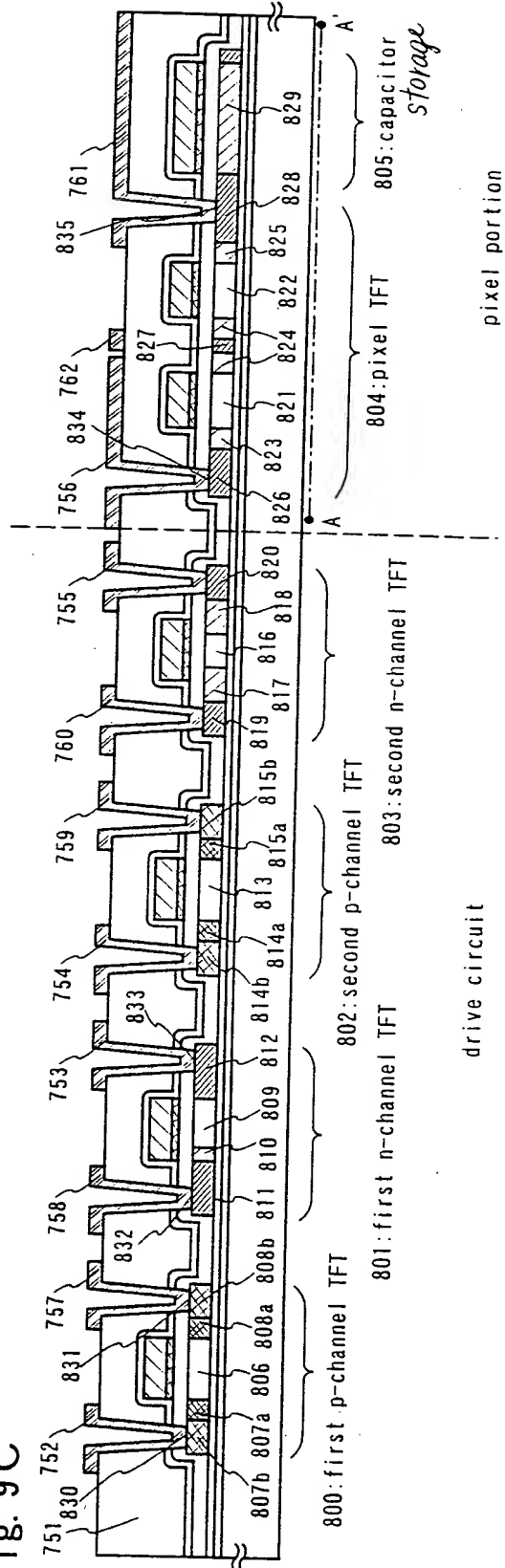


Fig. 10A

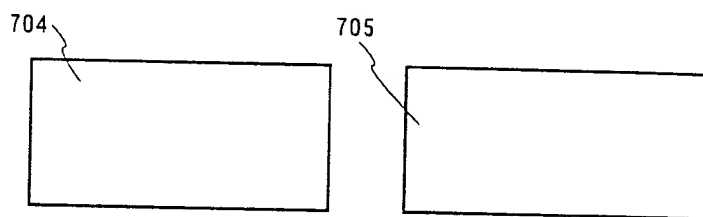


Fig. 10B

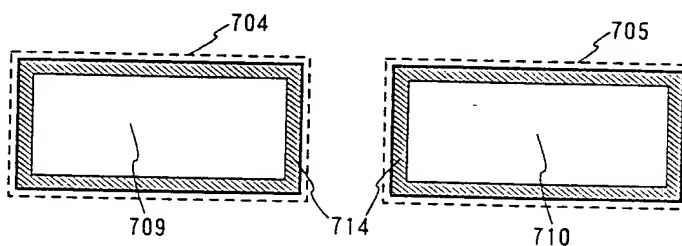


Fig. 10C

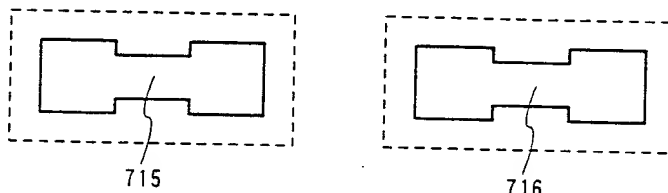


Fig. 10D

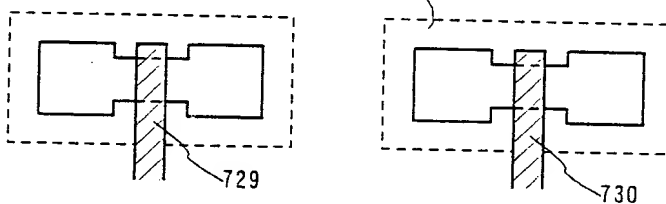


Fig. 10E

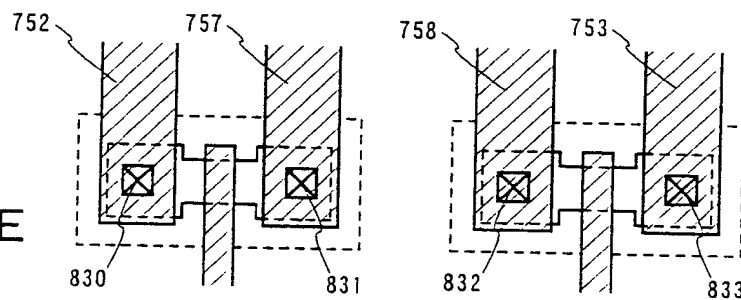


Fig. 11A

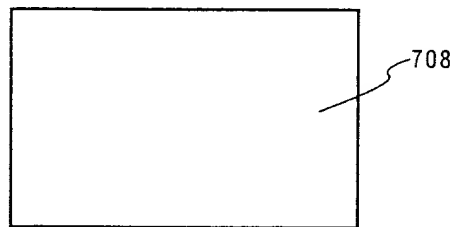


Fig. 11B

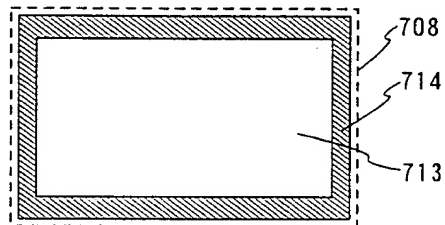


Fig. 11C

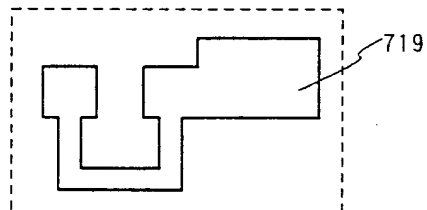


Fig. 11D

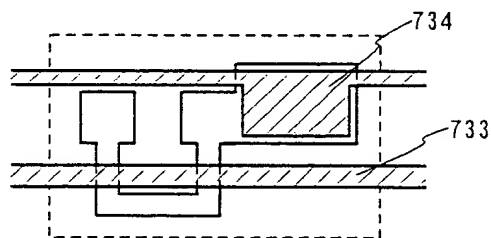
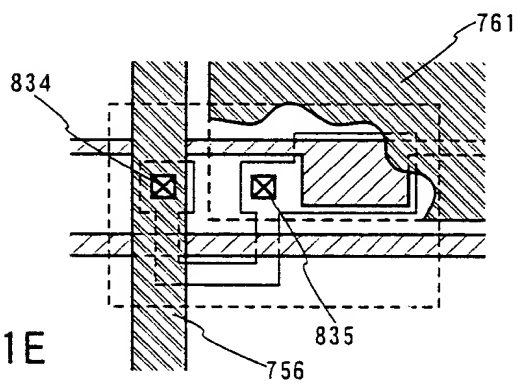


Fig. 11E



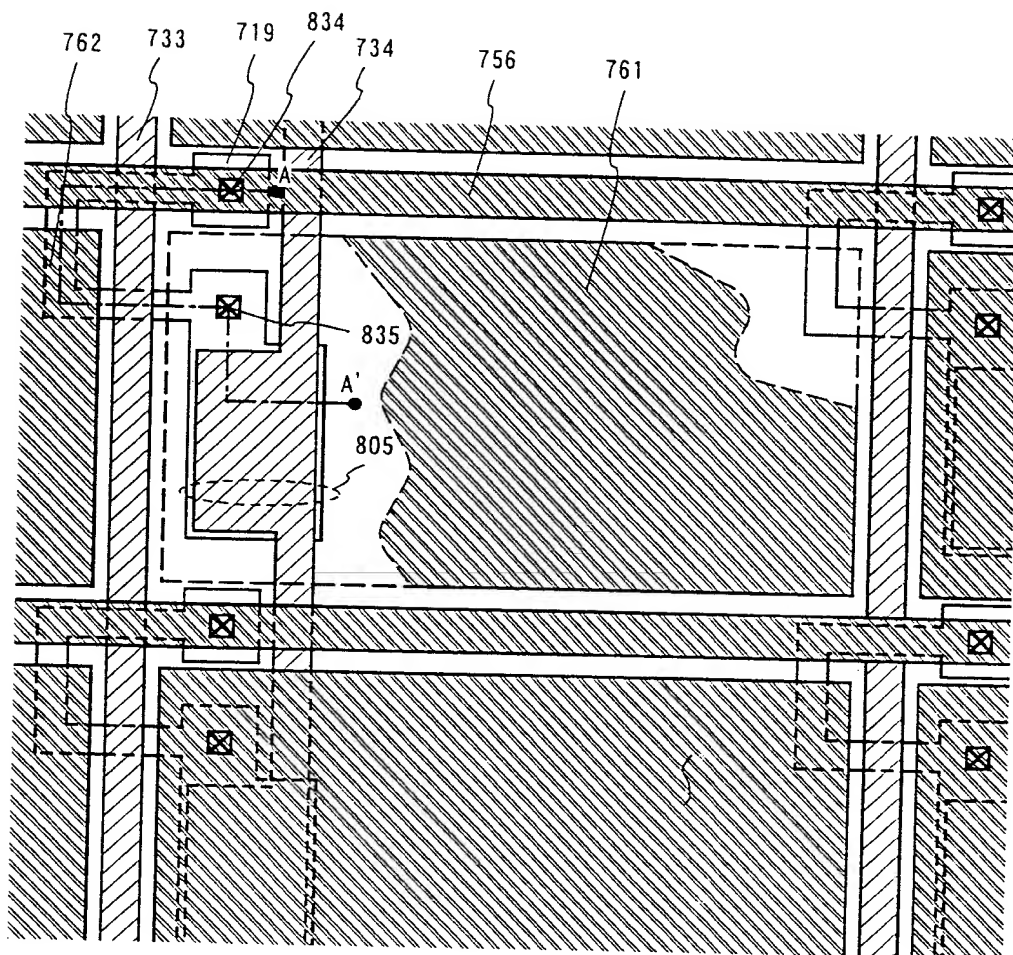


Fig. 12

FIG. 13A is a cross-sectional view of a semiconductor device in accordance with one embodiment of the present invention. The device includes a substrate 901a, a gate stack 901b, a gate stack 901c, a gate stack 901d, a gate stack 901e, a gate stack 901f, and a gate stack 902. The gate stacks are arranged in a row and are separated by a gate spacer 901g. The gate stacks are formed on a substrate 901a. The gate stack 901b is formed on a substrate 901a. The gate stack 901c is formed on a substrate 901a. The gate stack 901d is formed on a substrate 901a. The gate stack 901e is formed on a substrate 901a. The gate stack 901f is formed on a substrate 901a. The gate stack 902 is formed on a substrate 901a.

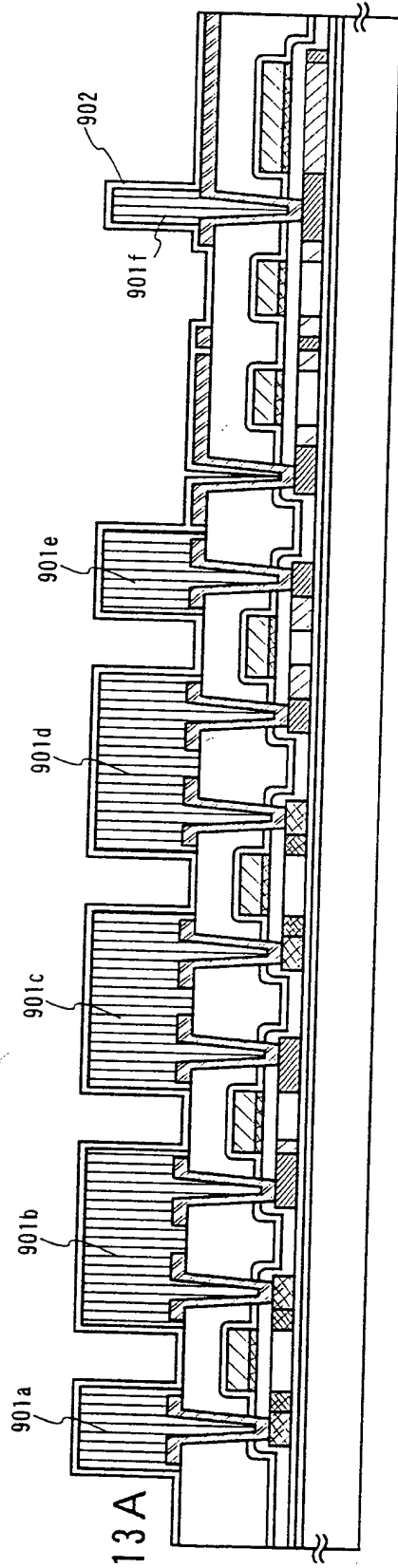
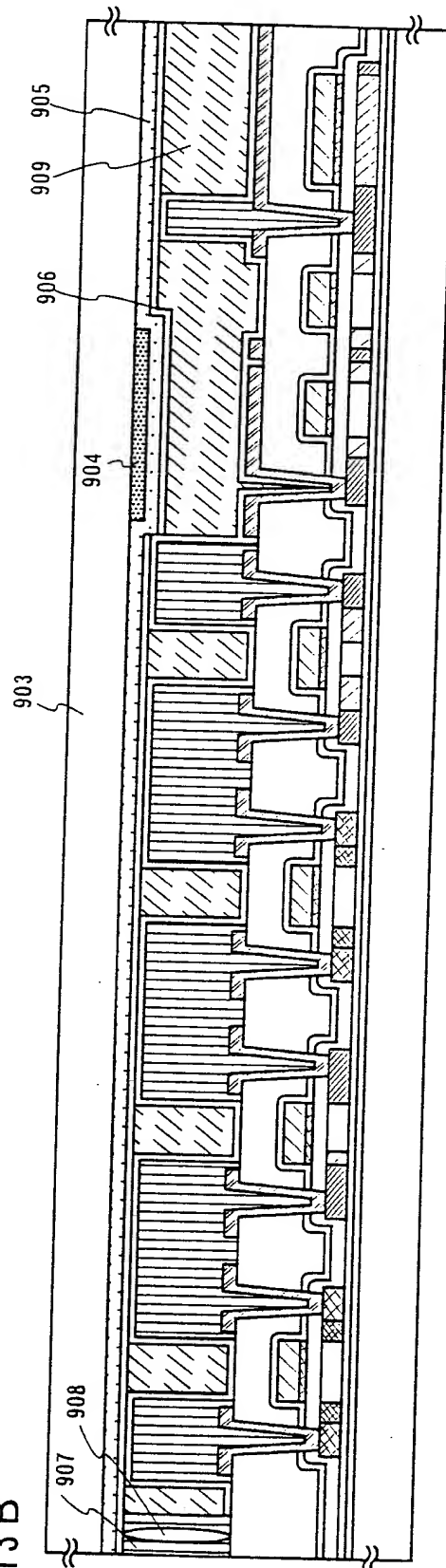


Fig. 13A

Fig. 13B



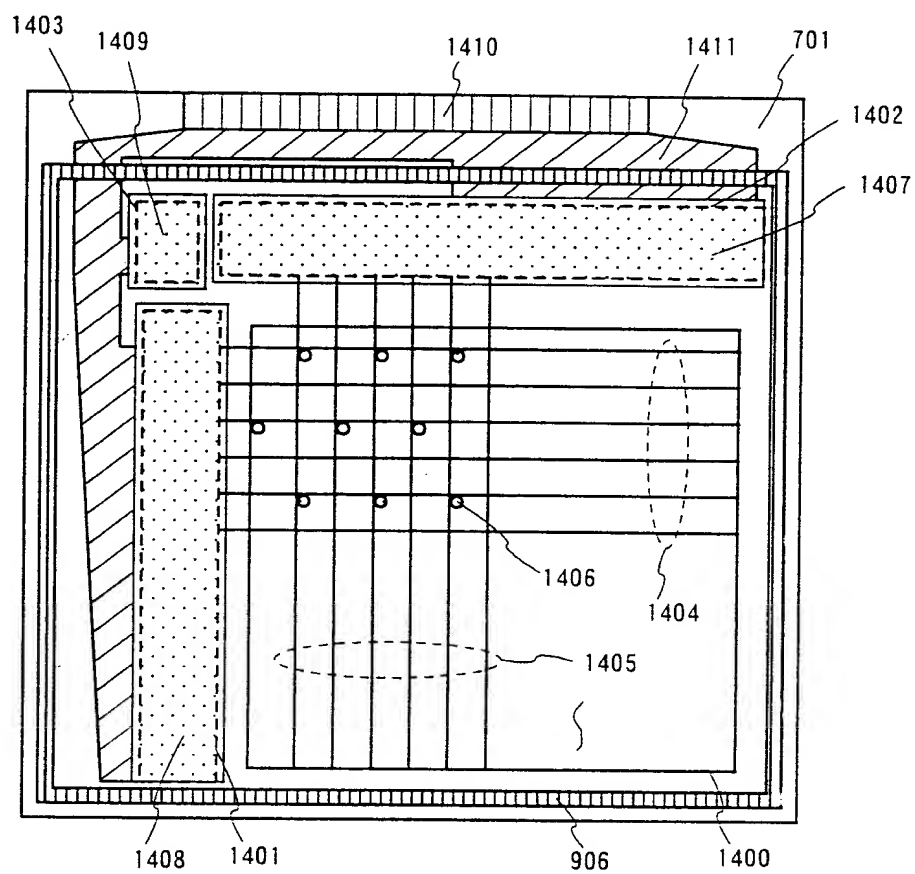


Fig. 14

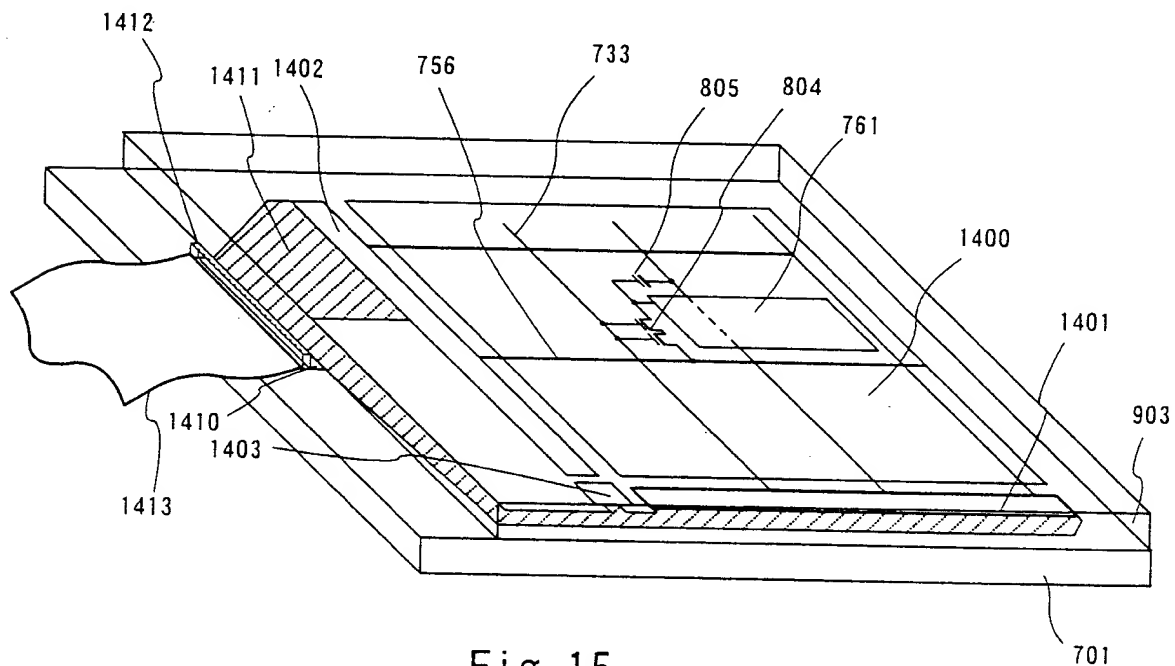


Fig. 15

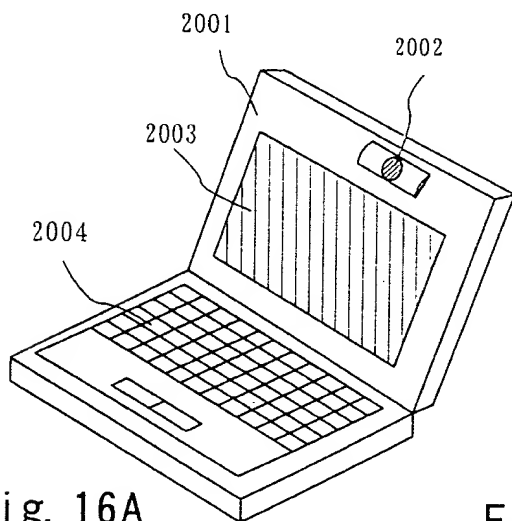


Fig. 16A

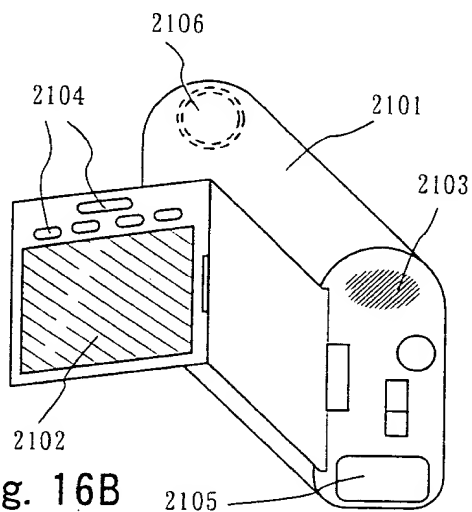


Fig. 16B

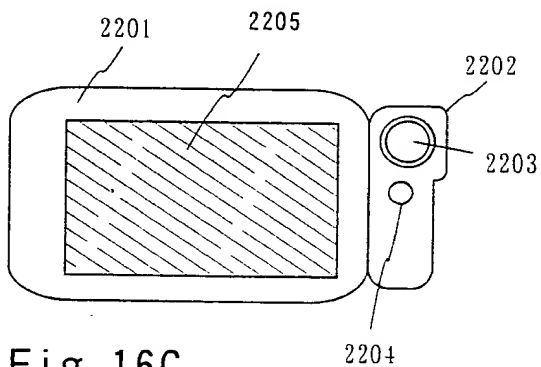


Fig. 16C

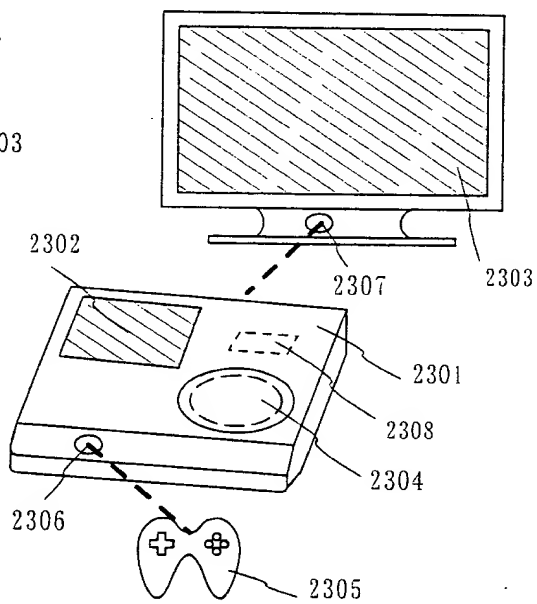


Fig. 16D

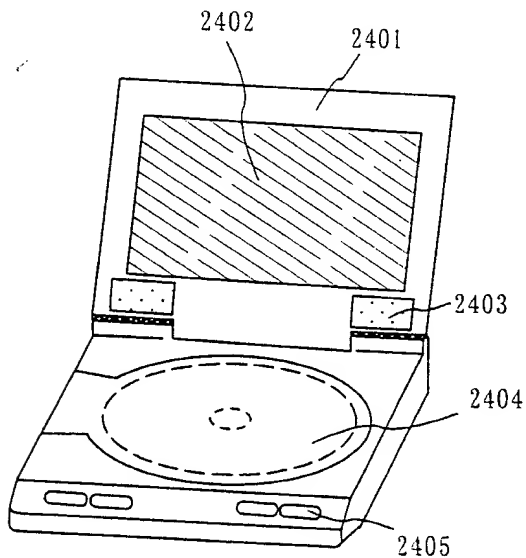


Fig. 16E

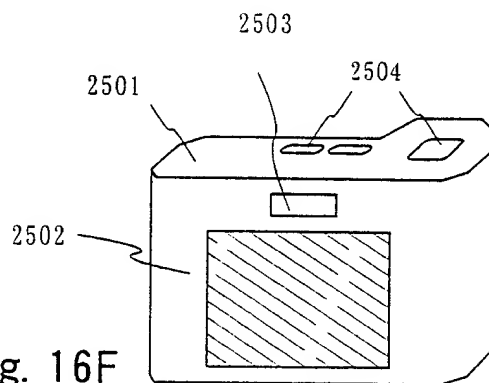


Fig. 16F

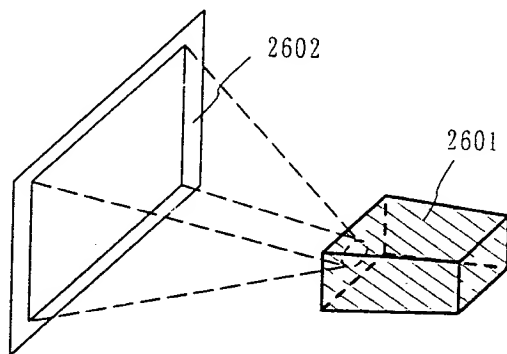


Fig. 17A

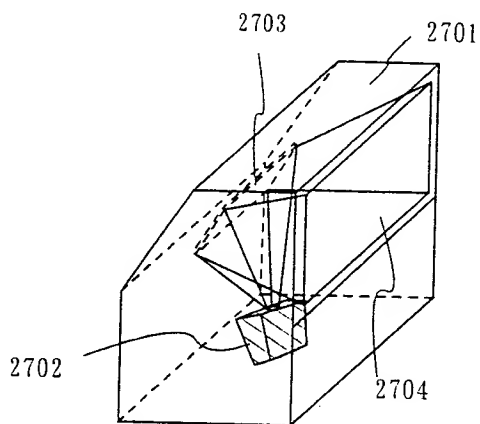


Fig. 17B

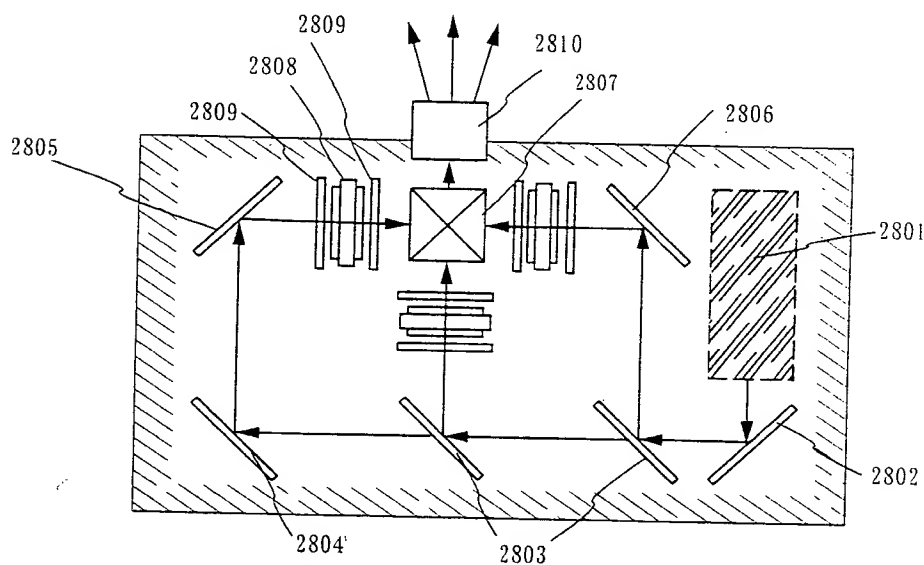


Fig. 17C

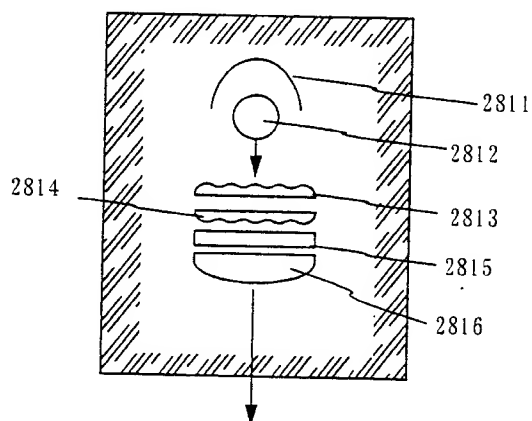


Fig. 17D

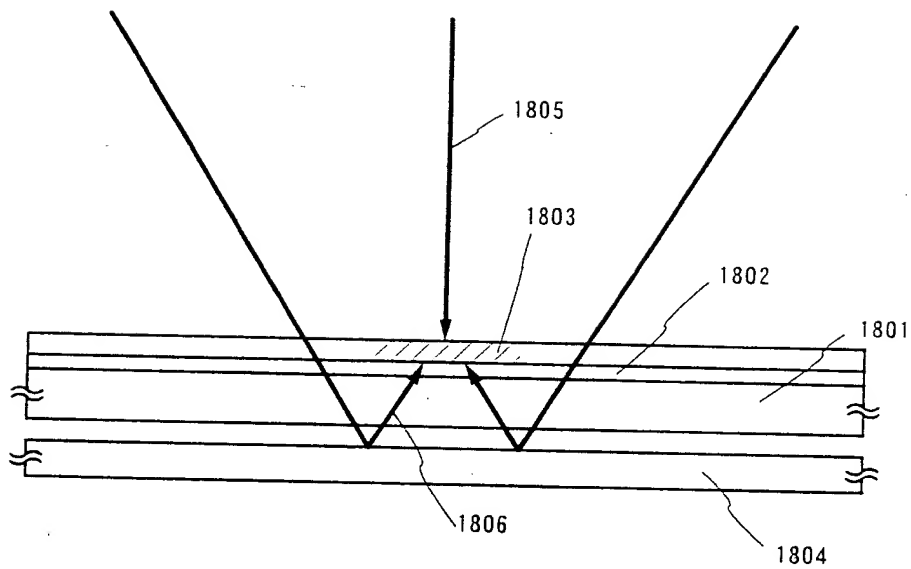


Fig. 18